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Appl. No. 10/707,647
Amdt. dated August 23, 2006
Reply to Office action of June 16, 2006

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

- 1 (currently amended): A high ~~voltage power~~ auto selecting circuit comprising:
- 5 a first transistor where a first terminal of the first transistor ~~being is~~ electrically coupled to a first ~~voltage power~~, a second terminal of the first transistor ~~being is~~ electrically coupled to an output node, and a gate of the first transistor ~~being is~~ electrically coupled to a second ~~voltage power~~; and
- 10 a second transistor where a first terminal of the second transistor ~~being is~~ electrically coupled to the second ~~voltage power~~, a second terminal of the second transistor ~~being is~~ electrically coupled to the output node, and a gate of the second transistor ~~being is~~ electrically coupled to the first ~~voltage power~~;
- 15 wherein the high ~~voltage power auto~~ selecting circuit selectively generates an output voltage according to a higher one of the voltages output by the first voltage power and the second ~~voltage power automatically, and the first power and the second power are~~ external power sources.
- 2 (currently amended): The high ~~voltage power auto~~ selecting circuit in claim 1, wherein the first transistor is a p-type MOS transistor and the first terminal of the first transistor is
- 20 a source and the second terminal of the first transistor is a drain.
- 3 (currently amended): The high ~~voltage power auto~~ selecting circuit in claim 1, wherein the second transistor is a p-type MOS transistor and the first terminal of the second transistor is a source and the second terminal of the second transistor is a drain.
- 25 4 (currently amended): The high ~~voltage power auto~~ selecting circuit in claim 1, wherein the first transistor further comprising a well and the well is electrically coupled to the

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second terminal of the first transistor.

5 (currently amended): The high ~~voltage power~~ auto selecting circuit in claim 1, wherein the second transistor further comprising a well and the well is electrically coupled to the
5 second terminal of the second transistor.

6 (currently amended): The high ~~voltage power~~ auto selecting circuit in claim 1, wherein
when an absolute value of a difference between the voltages output by the first voltage
power and the second voltage power is larger than a threshold voltage of the first and
10 second transistors, and the output voltage is substantially a higher one of voltage output
by the first voltage power and the second voltage power.

7 (currently amended): The high ~~voltage power~~ auto selecting circuit in claim 1, wherein
when an absolute value of a difference between the voltages output by the first voltage
15 power and the second voltage power is smaller than a threshold voltage of the first and
second transistors, and the output voltage is substantially the higher one of the voltage
output by the first voltage power and the second voltage power subtracting an minus a
junction voltage between the first terminal and the well of the first transistor or the second
transistor.

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8 (currently amended): A power supply voltage switching circuit for selecting a power supply voltage for an integrated circuit according to a first control signal, the circuit comprising:

25 a high voltage selecting module for generating an output voltage according to a
higher one of a voltage output by a first voltage power and a voltage output by a second
voltage power, the high voltage selecting module comprising:

a first transistor where a first terminal of the first transistor is electrically
coupled to the first power, a second terminal of the first transistor is electrically

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- coupled to an output node, and a gate of the first transistor is electrically coupled to the second power; and
- a second transistor where a first terminal of the second transistor is electrically coupled to the second power, a second terminal of the second transistor is
- 5 electrically coupled to the output node, and a gate of the second transistor is electrically coupled to the first power;
- wherein the high voltage selecting module selectively generates an output voltage according to a higher voltage output by the first power and the second power automatically, and the first power and the second power are external power sources;
- 10 a level shifting module electrically coupled to the high voltage selecting module for inputting the output voltage as a power supply of the level shifting module, for performing level shift on the first control signal according to the output voltage; and
- a selecting switch module electrically coupled to the level shifting module, for selectively outputting the voltage output by the first voltage power or the voltage output
- 15 by the second voltage power as the power supply voltage of the integrated circuit according to the level-shifted first control signal.

9 (cancelled).

- 20 10 (currently amended): The circuit in ~~claim 9~~ claim 8, wherein the first transistor is a p-type MOS transistor and the first terminal of the first transistor is a source and the second terminal of the first transistor is a drain.

- 25 11 (currently amended): The circuit in ~~claim 9~~ claim 8, wherein the second transistor is a p-type MOS transistor and the first terminal of the second transistor is a source and the second terminal of the second transistor is a drain.

12 (currently amended): The circuit in ~~claim 9~~ claim 8, wherein the first transistor further

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comprises a well and the well is electrically coupled to the second terminal of the first transistor.

13 (currently amended): The circuit in ~~claim 9~~ claim 8, wherein the second transistor
5 further comprises a well and the well is electrically coupled to the second terminal of the second transistor.

14 (currently amended): The circuit in ~~claim 9~~ claim 8, wherein when an absolute value
of a difference between the voltages output by the first voltage power and the second
10 voltage power is larger than a threshold voltage of the first and second transistors, and the
output voltage is substantially the higher voltage output by one of the first voltage power
and the second voltage power.

15 (currently amended): The circuit in ~~claim 9~~ claim 8, wherein when an absolute value
15 of a difference between the voltages output by the first voltage power and the second
voltage power is smaller than a threshold voltage of the first and second transistors, and
the output voltage is substantially the higher voltage output by one of the first voltage
power and the second voltage power subtracting an minus a junction voltage between the
first terminal and the well of the first transistor or the second transistor.

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16 (original): The circuit in claim 8, wherein the level shifting module further performs
level shift on a second control signal according to the output voltage and the second
control signal is complementary to the first control signal.

25 17 (currently amended): The circuit in claim 16, wherein the selecting switch module
further comprises:

a third transistor where a first terminal of the third transistor ~~being~~ is electrically
coupled to the first voltage power, a second terminal of the third transistor ~~being~~ is

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electrically coupled to a supply node, and the gate of the third transistor ~~being~~ is electrically coupled to the level-shifted first control signal; and

- 5 a fourth transistor where a first terminal of the fourth transistor ~~being~~ is electrically coupled to the second ~~voltage~~ power, a second terminal of the fourth transistor ~~being~~ is electrically coupled to the supply node, and a gate of the fourth transistor ~~being~~ is electrically coupled to the level-shifted second control signal;

wherein the selecting switch module generates the power supply voltage for the integrated circuit at the supply node according to the level-shifted first and second control voltage.

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18 (original): The circuit in claim 17, wherein the third transistor is a p-type MOS transistor and the first terminal of the third transistor is a source and the second terminal of the third transistor is a drain.

- 15 19 (original): The circuit in claim 17, wherein the fourth transistor is a p-type MOS transistor and the first terminal of the fourth transistor is a source and the second terminal of the fourth transistor is a drain.

- 20 20 (new): The high power auto selecting circuit in claim 1 wherein the voltages output by the first power and the second power are not related to one another in any way.

21 (new): The circuit in claim 8 wherein the voltages output by the first power and the second power are not related to one another in any way.